CLAIMS

I claim:

1. An integrated circuit comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure,

wherein the multi-layer structure includes a semiconductor substrate overlaid with a plurality of epitaxial semiconductor common to the D-mode and E-mode FETs, including a channel layer overlaid by a barrier layer overlaid by a first layer,

wherein the D-mode and E-mode FETs each include a source contact, a drain contact, and a gate contact, and

wherein the respective source and drain contacts of the D-mode FET and E-mode FET are coupled to the first layer, and the respective gate contacts of the D-mode FET and E-mode FET are coupled to the barrier layer.

2. The integrated circuit of claim 1, further comprising a solid state amorphization region beneath the E-mode gate contact at least within the barrier layer.

3. The integrated circuit of claim 2, wherein the solid state amorphization region includes at least one compound including at least one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium.

4. The integrated circuit of claim 2, wherein the solid state amorphization region includes a plurality of compounds, wherein at least one of the compounds includes

one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium, and at least one of the compounds includes a different one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium.

5. The integrated circuit of claim 2, wherein the multi-layer structure further comprises at least an epitaxial second layer between the barrier layer and the first layer.

6. The integrated circuit of claim 2, wherein the barrier layer is of a first conductivity type; and

further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact,

wherein the solid state amorphization region is within the implant region.

7. An integrated circuit comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure,

wherein the multi-layer structure includes a semiconductor substrate overlaid with a plurality of epitaxial semiconductor layers common to the D-mode and E-mode FETs, including a channel layer overlaid by a barrier layer overlaid by a first layer overlaid by a second layer,

wherein the D-mode and E-mode FETs each include a source contact, a drain contact, and a gate contact, and

wherein the source and drain contacts of the D-mode FET and the E-mode FET are coupled to the second layer,

wherein the gate contact of the D-mode FET is coupled to the first layer, and a solid state amorphization region is beneath the D-mode gate contact within the first layer, and

wherein the gate contact of the E-mode FET is coupled to the barrier layer, and a solid state amorphization region is beneath the E-mode gate contact within the barrier layer.

8. The integrated circuit of claim 7, wherein the multi-layer substrate includes an epitaxial third layer between the first layer and the barrier layer, said third layer having a different composition than the first layer and the barrier layer, and

wherein the D-mode solid state amorphization region is within the third layer.

9. The integrated circuit of claim 7, wherein the barrier layer is of a first conductivity type; and

further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact,

wherein the E-mode solid state amorphization region is within the implant region.

10. The integrated circuit of claim 7, wherein the D-mode and E-mode solid state amorphization regions include at least one compound including platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium.

11. The integrated circuit of claim 7, wherein the at least one of the D-mode and E-mode solid state amorphization

regions includes a plurality of compounds, wherein at least one of the compounds includes one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium, and at least one of the compounds includes a different one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium, rodium, and rhenium.

12. An integrated circuit comprising:

a depletion mode (D-mode) field effect transistor (FET) and an enhancement mode (E-mode) FET in a multi-layer structure,

wherein the multi-layer structure includes a semiconductor substrate overlaid with a plurality of epitaxial semiconductor layers common to the D-mode and E-mode FETs, including a channel layer overlaid by a barrier layer overlaid at least by a first layer;

wherein the D-mode and E-mode FETs each include a source contact, a drain contact, and a gate contact, and

wherein the source and drain contacts of the D-mode FET and the E-mode FET are coupled to one of the epitaxial layers overlying the channel layer,

wherein a gate contact of the D-mode FET is coupled to one of the first and barrier layers, and

wherein a gate contact of the E-mode FET is coupled to one of the first and the barrier layers, and

wherein a solid state amorphization region is present beneath the E-mode gate contact at least within the barrier layer.

13. The integrated circuit of claim 12, wherein the D-mode gate contact is coupled to the first layer, and the E-mode gate contact is coupled to the barrier layer.

14. The integrated circuit of claim 13, further comprising a second solid state amorphization region disposed beneath the D-mode gate contact at least within the first layer.

15. The integrated circuit of claim 12, wherein the D-mode and E-mode source and drain contacts are coupled to the first layer, and the D-mode and E-mode gate contacts are coupled to the barrier layer.

16. The integrated circuit of claim 12, wherein the D-mode and E-mode source and drain contacts are coupled to the first layer, and the E-mode gate contact is coupled to the barrier layer.

17. The integrated circuit of claim 12, wherein the barrier layer is of a first conductivity type; and

further comprising an implant region of a second conductivity type formed at least in the barrier layer beneath the E-mode gate contact,

wherein the E-mode solid state amorphization region is within the implant region.

18. A method of making an integrated circuit including a D-mode FET and an E-mode FET, the method comprising:

providing a multi-layer structure comprising a semiconductor substrate overlaid with a plurality of epitaxial semiconductor layers, including a channel layer

overlaid by a barrier layer, wherein the channel and barrier layers are common to the D-mode and the E-mode FETs;

forming respective source and drain contacts for the D-mode FET and E-mode FET on one of the epitaxial layers of the multi-layer substrate;

forming a gate recess in the multi-layer structure for the D-mode FET, and a gate recess in the multi-layer structure for the E-mode FET, wherein a surface of the barrier layer is exposed at a bottom of the both the D-mode and E-mode gate recesses; and

depositing a plurality of metal layers onto the exposed surface of the barrier layer within the D-mode and E-mode gate recesses, thereby forming a D-mode gate contact and an E-mode gate contact,

wherein a first metal layer deposited in contact with the barrier layer in the D-mode gate recess is different than a first metal layer deposited in contact with the barrier layer in the E-mode gate recess.

19. The method of claim 18, further comprising:

fully amorphizing the first metal layer deposited in contact with the barrier layer in the E-mode gate recess into the barrier layer, wherein the first metal layer deposited in contact with the exposed surface of the barrier layer in the D-mode gate recess is not significantly amorphized into the barrier layer.

20. The method of claim 19, wherein the first metal layer deposited in contact with the exposed surface of the barrier layer in the E-mode gate recess comprises one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium, and the first metal

layer deposited in contact with the barrier layer in the D-mode gate recess is not one of iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium.

21. The method of claim 19, wherein the barrier layer is of a first conductivity type; and

further comprising forming an implant region of a second conductivity type at least in the barrier layer beneath the E-mode gate contact,

wherein the first metal layer of the E-mode gate contact is amorphized into the implant region.

22. The method of claim 18, wherein the first metal layer deposited in contact with the exposed surface of the barrier layer in the E-mode gate recess comprises one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium; and further comprising:

depositing a second metal layer on the E-mode first metal layer, wherein the second metal layer is a different one of platinum, iridium, palladium, nickel, cobalt, chromium, ruthenium, osmium rodium, and rhenium than the first metal layer; and

fully amorphizing second metal layer of the E-mode gate contact into the barrier layer.

23. A method of making an integrated circuit including a D-mode FET and an E-mode FET, the method comprising:

providing a multi-layer structure comprising a semiconductor substrate that is overlaid with a plurality of epitaxial semiconductor layers, including a channel layer overlaid by a barrier layer overlaid by a first layer

overlaid by an second layer, wherein the channel layer, the barrier layer, and the first and second layers are common to the D-mode and E-mode FETs;

forming respective source and drain contacts for the D-mode FET and the E-mode FET on the second layer;

etching a gate recess into the multi-layer structure for the D-mode FET, wherein a surface of the first layer is exposed at a bottom of the D-mode gate recess;

etching a gate recess into the multi-layer structure for the E-mode FET, wherein a surface of the barrier layer is exposed at a bottom of the E-mode gate recess;

depositing a plurality of metal layers onto the exposed surface of the first layer within the D-mode gate recess, thereby forming a D-mode gate contact, wherein a first metal layer of the plurality of metal layers is in contact with the exposed surface of the first layer;

depositing a plurality of metal layers onto the exposed surface of the barrier layer within the E-mode gate recess, thereby forming an E-mode gate contact, wherein a first metal layer of the plurality of metal layers is in contact with the exposed surface of the barrier layer;

fully amorphizing the first metal layer of the D-mode gate contact into the multi-layer structure, thereby forming an amorphized region at least in the first layer beneath the D-mode gate contact; and

fully amorphizing the first metal layer of the E-mode gate contact into the multi-layer structure, thereby forming an amorphized region at least in the barrier layer beneath the E-mode gate contact.

24. The method of claim 23, wherein the multi-layer substrate includes an epitaxial third layer composed of a

material different from the first layer and the barrier layer, the third layer being disposed between the first layer and the barrier layer beneath the D-mode and E-mode gate contacts, and the amorphized region beneath the D-mode gate contact extends into the second layer.

25. The method of claim 23, wherein the barrier layer is of a first conductivity type; and

further comprising forming an implant region of a second conductivity type at least in the barrier layer beneath the E-mode gate contact,

wherein the first metal layer of the E-mode gate contact is amorphized into the implant region of the barrier layer.

26. A method of making an integrated circuit including a D-mode FET and an E-mode FET, the method comprising:

providing a multi-layer structure comprising a semiconductor substrate overlaid with a plurality of epitaxial semiconductor layers, including at least a channel layer overlaid by a barrier layer, wherein at least the channel and barrier layers are common to the D-mode and the E-mode FETs;

forming respective source and drain contacts for the D-mode FET and E-mode FET on the multi-layer substrate over the barrier layer;

forming a gate recess in the multi-layer structure for the E-mode FET, wherein a surface of the barrier layer is exposed at a bottom of the E-mode gate recess;

depositing a plurality of metal layers onto the multi-layer substrate to form a D-mode gate contact;

depositing a plurality of metal layers onto the exposed surface of the barrier layer within the E-mode gate recess, thereby forming an E-mode gate contact, wherein the plurality of metal layers includes a first metal layer in contact with the exposed surface of the barrier layer;.

fully amorphizing the first metal layer of the E-mode gate contact into the barrier layer, wherein a first metal layer of the D-mode gate contact that was deposited in contact with the multi-layer substrate is not significantly amorphized into the multi-layer substrate.

27. The method of claim 26, further comprising:

forming a gate recess in the multi-layer structure for the D-mode FET, wherein a surface of the barrier layer is exposed at a bottom of the D-mode gate recess,

wherein the first metal of the D-mode gate contact is in contact with the barrier layer.